WHAT IS CLAIMED IS:

1. A data processor having an SIMD type execution unit:

said data processor having an instruction to cause said SIMD type execution unit to process vector data.

2. A data processor, as claimed in Claim 1, wherein:

said SIMD type execution unit has a plurality of execution units for performing multiply-add operations on floating-point numbers.

3. A data processor for executing instructions in an instruction set and having an SIMD type execution unit, wherein:

said instruction set includes an instruction for causing said SIMD type execution unit to operate on vector data.

4. A data processor, as claimed in Claim 3, wherein:

said SIMD type execution unit has a plurality of execution units for performing multiply-add operations on floating-point numbers.

5. A data processor for executing instructions in an instruction set, wherein:

said instruction set includes an instruction for causing said data processor to calculate the sum of the inner product of vectors and scalar data.

6. A data processor, as claimed in Claim 5:

said data processor having a floating-point execution unit for calculating the inner product of a length-4 vector and another length-4 vector and the sum of said product and scalar data.

7. A data processor, as claimed in Claim 6, wherein:

said floating-point execution unit has a 9 input adder.

8. A data processor for executing instructions in an instruction set, wherein:

said instruction set includes an instruction for causing said data processor to calculate the product of matrix data and vector data.

9. A data processor, as claimed in Claim 8:

said data processor having a plurality of floating-point execution units for calculating the inner product of a vector and another vector.

10. A data processor, as claimed in Claim 8, wherein:

said matrix data are 4 × 4 matrix data and said vector data are length-4 vectors.

11. A data processor, as claimed in Claim 9, wherein:

each of said plurality of floating-point execution units is an execution unit capable of calculating the sum of said inner product and scalar data.

12. A data processing system, as claimed in Claim 11, wherein:

said execution unit has a 9 input adder.